Sub C3 B3 cont.

an inter-poly dielectric layer over said floating Poly-Si gate; ~~and~~

a Poly-Si control gate over said ~~inter-poly~~ dielectric layer.

B4 Sub D2

3. (AMENDED) A stacked-gate flash memory cell of claim 1, wherein said regions of different cross-sectional shapes have a depth between about 900 to 1100 Å.

Claim 4, please cancel.

REMARKS

Claims 1-3 and claims 5, 6 remain in this application. Claim 1 has been amended, and claim 4 cancelled.

Examiner Thomas L. Dickey is thanked for having thoroughly examined the present invention.

The applicants also thank the examiner for indicating condition for allowance.

Following the suggestion of the examiner, a new drawing is being submitted, with no new matter, in order to illustrate the claims of the invention. Examiner's approval is requested, respectfully.

A claim to domestic priority has also been entered as per request from the examiner.

In claim 1, the word "providing" has been cancelled, and it is believed that objection to claims 1-6 has now been overcome, and it is so requested, respectfully.

Reconsideration of the rejection of claims 1-6 under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention, is respectfully requested in view of the amendments and for the reasons given below.

As the examiner correctly points out, what was meant in claims 1-6 was insufficient to cite the meaning that the

surfaces were the outer boundaries of regions having certain cross-sectional areas. Accordingly, claims 1 and 3 have been amended to particularly point out the cross-sections underlying the respective surfaces. Claim 4 has been incorporated into claim with the proper Markush language and cancelled. With these corrections, it is believed that the claims 1-6 are now allowable, and it is so requested, respectfully.

Reconsideration of the rejection of claim 1 under 35 USC 102(a) as being anticipated by ARAI (6,329,688) is respectfully requested in view of the amendments and for the reasons given below.

Claim 4 with allowable subject matter has been incorporated in claim 1. It is believed that claim 1 is now allowable, and it is so requested, respectfully.

Reconsideration of the rejection of claims 2, 3, 5 and 6 under 35 USC 103(a) as being unpatentable over ARAI (6,329,688)is respectfully requested in view of the amendments and for the reasons given below.

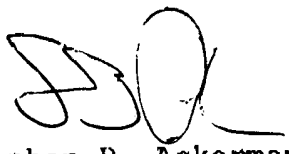
Claim 4 with allowable subject matter has been incorporated in claim 1. It is believed that claim 1 is now allowable, and, hence also claims dependent from claim 1, and it is so requested, respectfully.

Allowance of all claims, as amended, is requested.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. the attached page is captioned **"Version with Marking to Show Changes Made."**

It is requested that should the Examiner not find that the Claims Allowable that are now presented, that he call the undersigned Attorney at 845/452-5863 to overcome any problems preventing allowance.

Respectfully submitted,



Stephen B. Ackerman, Reg. No: 37,761

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

On page 1, after the title, the following claim to priority has been amended as follows:

This is a division of Patent Application serial number 09/347,547, filing date 7/6/99, Step-Shaped Floating Py-Si Gate To Improve Gate Coupling Ratio for Flash Memory Application, now U.S. Patent No. 6,225,162, assigned to the same assignee as the present invention.

On page 16, after the second paragraph ending with the words "45 KeV", a new paragraph has been entered as follows:

The process steps shown in Figures 2a-2l are also applicable to other surfaces of different shapes, as stated previously. Figure 2m shows the application to "folded" surfaces having regions with triangular cross-sections (205). Regions with other cross-sections can also be

formed, as well as a combination may be achieved through alternating layers with flat surfaces and folded regions having triangular cross-sections.

IN THE CLAIMS

The following claims have been amended as follows:

1. (AMENDED) A stacked-gate flash memory cell having a floating Poly-Si gate with multiply connected surfaces of different shapes comprising:

[providing] a semiconductor substrate;

a floating Poly-Si gate with multiply connected surfaces having regions of different cross-sectional shapes;

wherein said cross-sectional shapes are selected from a group consisting of rectangular and triangular shapes;

an inter-poly dielectric layer over said floating Poly-Si gate; and

a Poly-Si control gate over said inter-poly dielectric layer.

3. (AMENDED) A stacked-gate flash memory cell of claim 1, wherein said [multiply connected surfaces] regions of different cross-sectional shapes have a depth between about 900 to 1100 Å.

Claim 4 has been cancelled.